

# RVX7050M VCXO

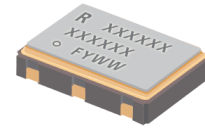
**rakon**

## SMD Voltage Controlled Crystal Oscillator

Ultra Low Noise VCXO in 7 x 5 mm Surface Mount Package.

### Product description

The RVX7050M is a very high performance VCXO delivering ultra low close-in phase noise for RF/Analog applications and ultra low RMS phase jitter optimised for high speed serial data and digital applications.



### Applications

- Communications
- Ethernet
- SONET/SDH
- DSL/ADSL
- Basestation
- WiFi
- WiMAX/WLAN

### Features

- Ultra Low Jitter 0.05 to 0.3 ps integrated 12 kHz to 20 MHz
- Excellent close-in phase noise performance
- LVCMOS, LVPECL, or LVDS Output options
- Wide frequency range

### Specifications

#### 1.0 SPECIFICATION REFERENCES

Line	Parameter	Description
1.1	Model Description	RVX7050M VCXO
1.2	Reference Number	
1.3	Rakon Part Number	

#### 2.0 FREQUENCY CHARACTERISTICS

Line	Parameter	Test Condition	Value	Unit
2.1	Frequency		1 to 800	MHz
2.2	Operating Temperature Range		-40 to 85	°C
2.3	Frequency Stability	Including Temperature range, Supply variation, Load variation and 15 years aging at 25°C	±30 to 50	ppm
2.4	Temperature Stability	Temperature range only	±10 to 20	ppm

#### 3.0 POWER SUPPLY

Line	Parameter	Test Condition	Value	Unit
3.1	Supply Voltage (VDD)	With a tolerance of ±10%	3.3	V
3.2	Supply Voltage (VDD)	With a tolerance of ±5% (availability advised at time of inquiry)	2.5	V
3.3	Supply Current	For LVCMOS	1 to 40	mA
3.4	Supply Current	For LVPECL	40 to 120	mA
3.5	Supply Current	For LVDS	30 to 80	mA

#### 4.0 CONTROL VOLTAGE (VCO)

Line	Parameter	Test Condition	Value	Unit
4.1	Absolute Pull Range (APR)		±50 min	ppm
4.2	Total Pull Range	Frequency shift from minimum to maximum control voltage	100 to 250	ppm
4.3	Control Voltage	Nominal 1.65V	0 to 3.3	V
4.4	Linearity	Control voltage 0.3 to 3V	10 max	%
4.5	Slope	Positive only		
4.6	Modulation BW	Control voltage 0.3 to 3V	15 min	kHz
4.7	Input Impedance		0.1 to 10	MΩ

#### 5.0 OUTPUT CHARACTERISTICS - CMOS (UP TO 200 MHz)

Line	Parameter	Test Condition	Value	Unit
5.1	Output Voltage (Vol)	10pF load	10 max	%VDD
5.2	Output Voltage (Voh)	10pF load	90 min	%VDD
5.3	Duty Cycle	@ 50% VDD	45 to 55	%
5.4	Rise Time/Fall Time	90%/10%	3 max	ns
5.5	RMS Phase Jitter	Typical integrated 12kHz to 20MHz	0.05 to 0.3	ps

#### 6.0 OUTPUT CHARACTERISTICS - LVPECL ONLY

Line	Parameter	Test Condition	Value	Unit
6.1	Output Voltage (Vol)	50Ω nominal load. (VDD - 1.6V) max.		
6.2	Output Voltage (Voh)	50Ω nominal load. (VDD - 1.03V) min.		
6.3	Duty Cycle	@ VDD-1.3V	45 to 55	%
6.4	Rise Time/ Fall Time	80%/20%	0.6 max	ns
6.5	RMS Phase Jitter	Typical integrated 12kHz to 20MHz	0.05 to 0.3	ps

#### 7.0 OUTPUT CHARACTERISTICS - LVDS ONLY

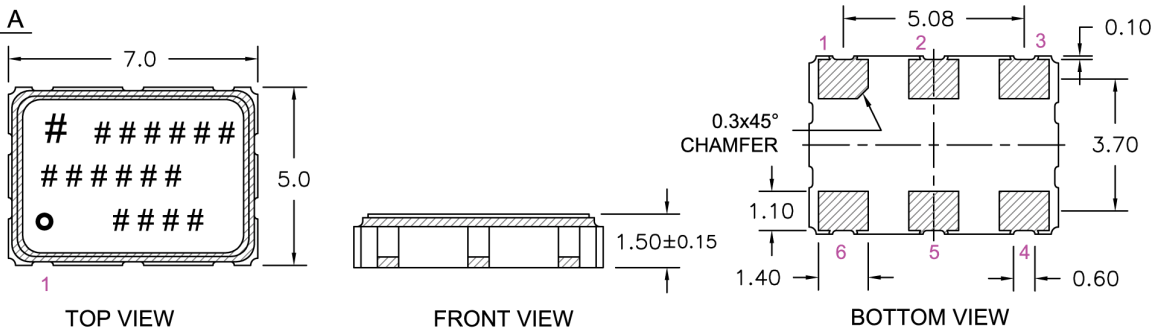
Line	Parameter	Test Condition	Value	Unit
7.1	Differential Output: Voltage Swing (Vod)		350	mV
7.2	Duty Cycle	Measured at 1.25 V	45 to 55	%
7.3	Rise Time/Fall Time	RL = 100 Ω / CL = 10 pF	0.6 max	ns
7.4	RMS Phase Jitter	Typical integrated 12kHz to 20MHz	0.05 to 0.3	ps

#### 8.0 SSB PHASE NOISE

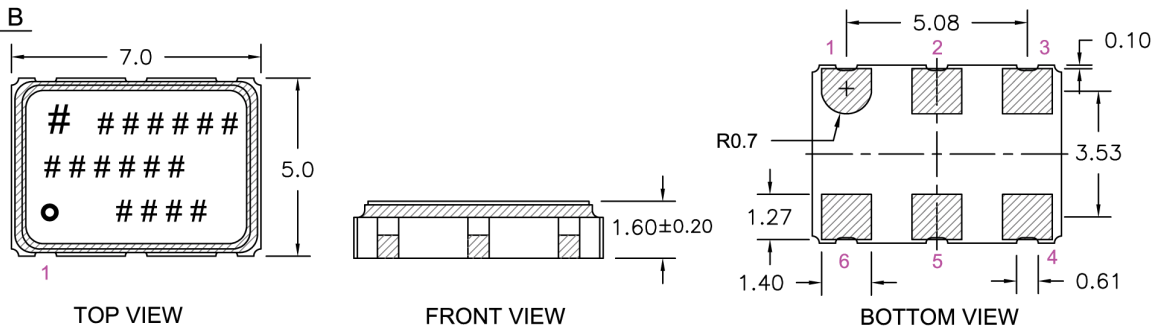
Line	Parameter	Test Condition	Value	Unit
8.1	SSB Phase Noise power density @ 10 Hz offset	Typical value for a 77.76 MHz VCXO @ 25 °C	-73	dBc/Hz
8.2	SSB Phase Noise power density @ 100 Hz offset	Typical value for a 77.76 MHz VCXO @ 25 °C	-100	dBc/Hz
8.3	SSB Phase Noise power density @ 1 kHz offset	Typical value for a 77.76 MHz VCXO @ 25 °C	-128	dBc/Hz
8.4	SSB Phase Noise power density @ 10 kHz offset	Typical value for a 77.76 MHz VCXO @ 25 °C	-137	dBc/Hz
8.5	SSB Phase Noise power density @ 100 kHz offset	Typical value for a 77.76 MHz VCXO @ 25 °C	-148	dBc/Hz

# Drawing Name: XO/VCXO 7050 Model Drawing

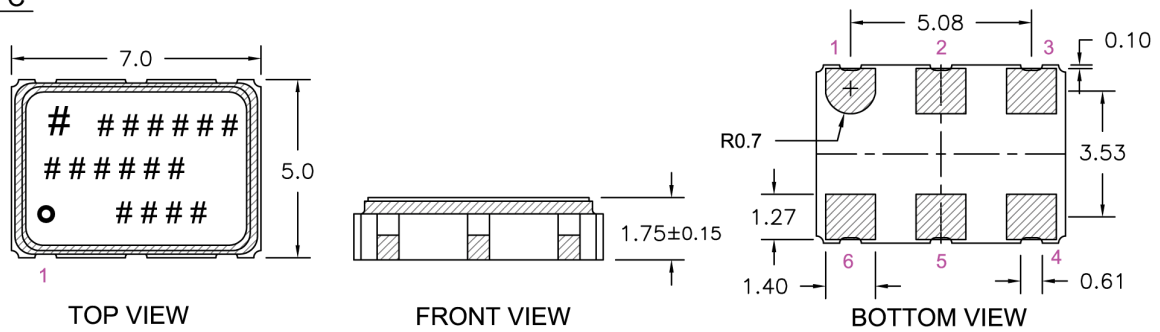
## PACKAGE A



## PACKAGE B

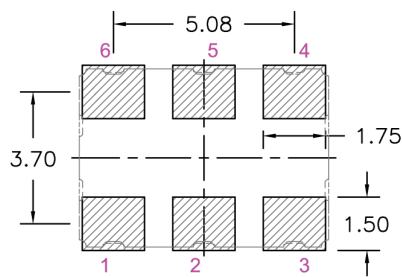


## PACKAGE C



## RECOMMENDED PAD LAYOUT

- TOP VIEW



### NOTE :

1. PIN CONNECTIONS ARE DETAILED IN THE SPECIFICATION.
2. MARKING INFORMATION IS DETAILED IN THE SPECIFICATION.

TITLE: XO/VCXO 7050 SERIES MODEL

FILENAME: CAT207

TOLERANCES:

RELATED DRAWINGS:

REVISION: J

XX =

DATE: 03-Apr-12

X.X = ±0.15

SCALE: 5 : 1

X.XX = ±0.10

Millimetres

X.XXX =

X° =

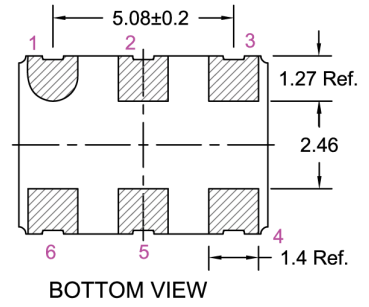
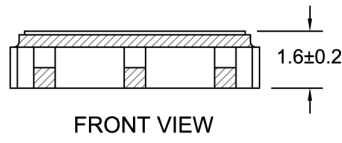
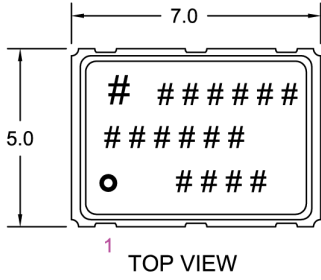
Hole =

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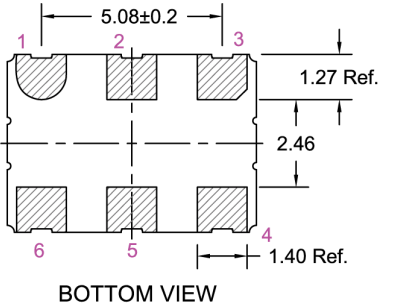
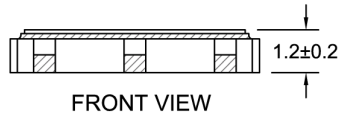
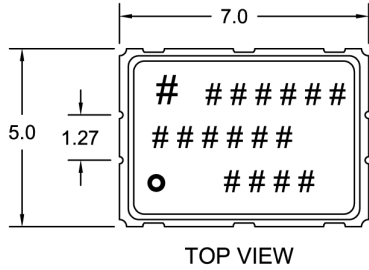
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# Drawing Name: XO/VCXO 7050 Alternate Model Drawing

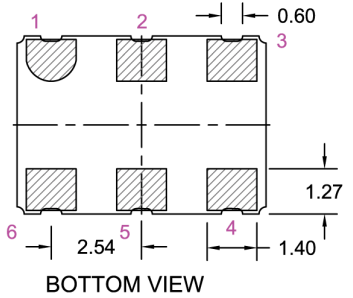
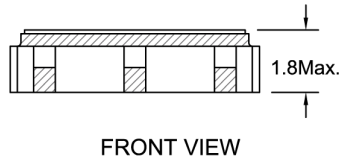
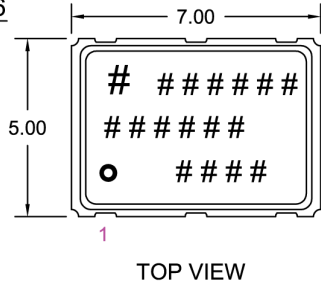
## PACKAGE GV



## PACKAGE G6



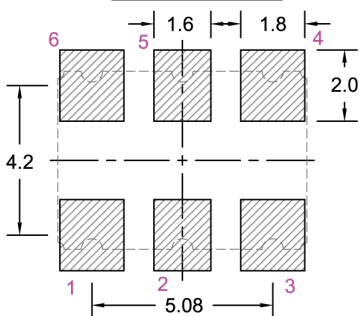
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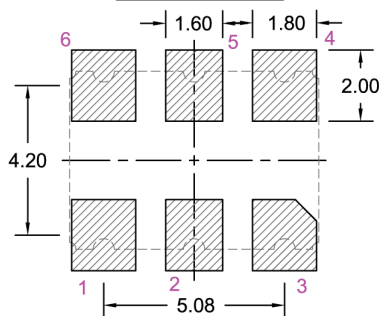
NOTE: 1. PIN CONNECTIONS ARE DETAILED IN THE SPECIFICATION.  
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## RECOMMENDED PAD LAYOUT - Top View

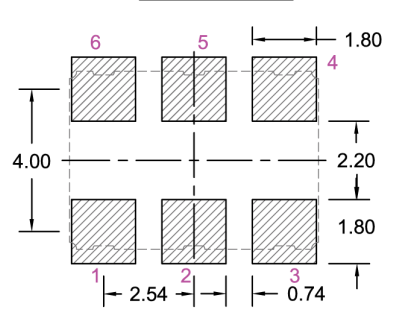
### PACKAGE GV



### PACKAGE G6



### PACKAGE J6



TITLE: XO/VCXO 7050 ALTERNATE MODEL

RELATED DRAWINGS:

FILENAME: CAT675

REVISION: C

DATE: 13-Apr-12

SCALE: 5 : 1

Millimetres

TOLERANCES:

XX =  
X.X = ±0.15  
X.XX = ±0.10  
X.XXX =  
X° =  
Hole =

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